
DISCLOSURE FORM FOLLOWS

DOCKET NO. TI _____

1. Please suggest a descriptive title for your invention:
Advanced IO architecture for Area-efficient (cost-efficient) system-on-a chip integration

2. What is the problem solved by your invention?

Traditional IO architecture (like 18C05's 75x188um² IO) can cause a wasted die area of 6-13% around IO periphery. The proposed super-short IO architecture utilize the area, hence reducing the silicon area by 6-13% or increase PFO by 6-13% for all WCBU products.

3. What is your solution to the problem?

- 1) Please refer to the foil attachment for super-short IO architecture for C035.

- 2) Traditional IO: 18C05 WCBU has achieved 75x188um² IO.

Proposed IO:

- o proposed the IO buffer/ESD area be next to the bondpad. This type of super-short/super-fat IO utilizes the typical "wasted area" typically seen in a core-limited design. One possible solution is 108x120um² C035 IO.

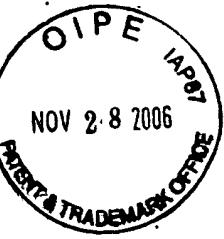
4. When was your solution first conceptually or mentally complete? Date: ____ / ____ / ____

5. What is the first tangible evidence of such completion?

Date: 01/06/99 presentation to Jeff Southard, Jeff Bellay, and briefing to Bobby Mitra.

6. What is different about your solution, compared with other solutions to the same problem?

- 1) Traditional IO like 75x188um² C05 IO grows in the



- Y-dimension due to bondpad, ESD, bussing, IO buffer. This wastes silicon area in the IO periphery for any core-limited design.
- 2) The proposed solution grows in X-dimension for IO buffer and busses in the vertical (M1/M2/M3/M4/M5/...) direction. This approach is especially desirable for 3G air-interface and applications chips where core-limited situation easily dominated due to complexity/functional increase.
- 3) The proposed solution also allow a hybrid growth in X- and Y-dimension to match the different core area (vs. IO area) and pin-count situation.
7. What are the advantages of your solution?
- 1) Save a typicalall 2/2.5G/3G wireless chip by area of 6-13% (see attached spreadsheet). This increases the PFO by up to 6-13%.
 - 2) The proposed solution is best optimized for 5-level metal process or more, though not absolutely demanding 5LM.
 - 3) The proposed solution can further reduce the power ring routing typically 50-100um
 - 4) Highly competitive solution which complements process technology
8. What TI products, processes, projects or operations currently implement your invention?
- 1) ASIC Backplane in GS40 product
 - 2) All WCBU DBB products starting from GS40: UFP, TIKU, MINI, WANDA, OMAP-based, . . . etc
9. What is the date of the first implementation?
1st Tapeout: _____
10. What record exists to prove this date?
Attached PowerPoint file presentation
11. Is there any future implementation planned? (Y/N)
If so, please furnish the TI PART No. or project name
See description in Item 8. above
12. Has the invention been published or disclosed to anyone outside of TI? (Y/N) _____ N _____ When? _____ If planned - when? _____ (Catalog, advertising, data book, application note, conference paper, magazine article, TI TJ, proposal document.) Was there a nondisclosure agreement (NDA)? (Y/N)

13. Has a TI product incorporating the invention been publicly introduced, quoted, sampled or shipped? (Y/N) N When? _____ If planned--when? _____

14. Was the invention conceived or first implemented in the performance of a government contract or subcontract? (Y/N) N Contract #: _____

THE INVENTION DESCRIBED BY THIS DISCLOSURE IS SUBMITTED PURSUANT TO
MY EMPLOYMENT AGREEMENT WITH TEXAS INSTRUMENTS INCORPORATED OR A TI
SUBSIDIARY (SPECIFY):

Has this disclosure been previously sent to the Patent Department electronically (unsigned)? (Y/N) _____
(Printed) Inventor 1: Uming Ko _____

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Phone #: (972) 480-6788 Country of Citizenship: USA
(Signed) L. Mitra _____ Date 8/22/23 Mail Station _____

This invention disclosure with any attachments was read and understood by me on 8/22/23.
Witness: Bobby Mitra _____ Date 8/22/23

This invention disclosure with any attachments was read and understood by me on 8/22/23.
Jeff Southard: _____

Witness 2

Date

This invention disclosure with any attachments was read and understood by me on 10/10/10.
Jeff Bellay:
Witness 3

Date

This invention disclosure with any attachments was read and understood by me on 10/10/10.

Witness 4

Date

*****END OF FORM*****



WCBU: IO Analysis & Status

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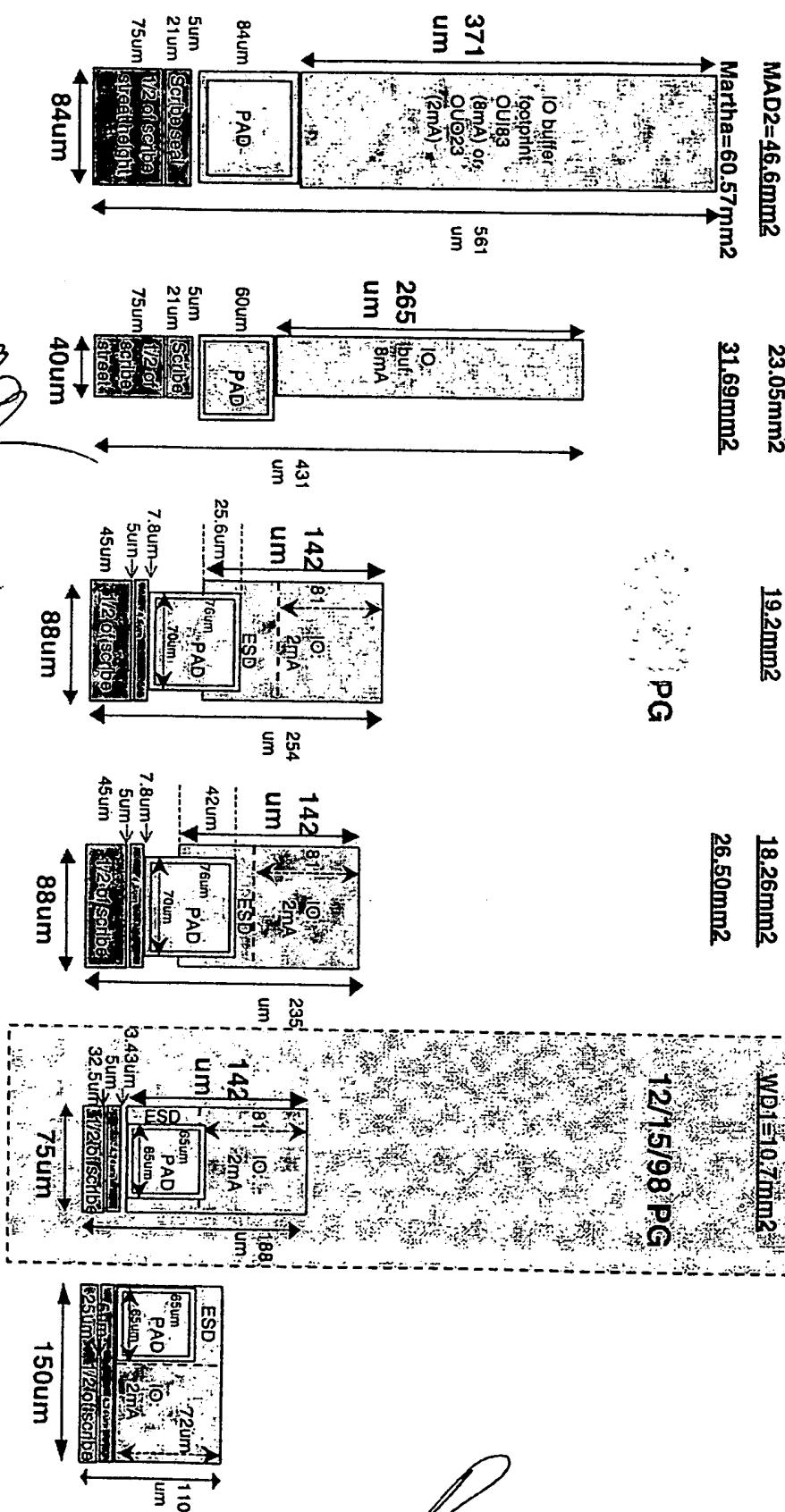
C07 ASIC(est)

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Entitlement 1833C07

1833C05
Entitlement

15C05/C35 Entitlement



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Wireless Communications Business Unit

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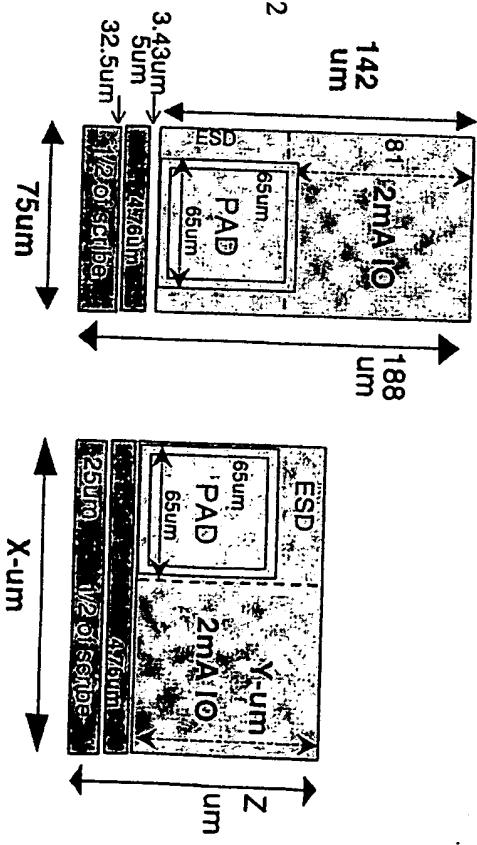


5LM Optimization Proposal: P.R./IO



- Power Ring around core:
 - Eliminate 50~100um ring in 5LM
 - Reduce chip area by x%
- 5LM IO footprint:

- Buffer+esd: $75 \times 142 \mu\text{m}^2 \Rightarrow 150 \times 72 \mu\text{m}^2$
- BOESD: remains at 100%
- Seal: remains at $4.76 \mu\text{m}$
- Scribe: $75 \mu\text{m} \Rightarrow 60 \mu\text{m}$
- Reduce chip area by x%



- Action: Wai/Steve/Don to confirm IO footprint feasibility by 11/20/06

C05: X=130, Y=82, Z=120
C35: X=108, Y=82, Z=120

UKO, 12

Wireless Communications Business Unit



TI PROPRIETARY INFORMATION - INTERNAL DATA

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Core area, mm ²	mm/side	IO type	IO height, um	IO width, um	Area	max IO	wasted area	UKO, % of chip
10	3.162	ASIC short IO	212	61	12.9	207	2.45	19%
		WCBU short-fat	188	75	12.5	169	1.67	13%
		WCBU super short-fat	120	108	11.6	117		
20	4.472	ASIC short IO	212	61	24.0	293	3.42	14%
		WCBU short-fat	188	75	23.5	239	2.33	10%
		WCBU super short-fat	120	108	22.2	166		
30	5.477	ASIC short IO	212	61	34.8	359	4.16	12%
		WCBU short-fat	188	75	34.3	292	2.83	8%
		WCBU super short-fat	120	108	32.7	203		
40	6.325	ASIC short IO	212	61	45.5	415	4.78	11%
		WCBU short-fat	188	75	44.9	337	3.26	7%
		WCBU super short-fat	120	108	43.1	234		
50	7.071	ASIC short IO	212	61	56.2	464	5.33	9%
		WCBU short-fat	188	75	55.5	377	3.63	7%
		WCBU super short-fat	120	108	53.5	262		
60	7.746	ASIC short IO	212	61	66.7	508	5.83	9%
		WCBU short-fat	188	75	66.0	413	3.97	6%
		WCBU super short-fat	120	108	63.8	287		

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